REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1, 3-4, and 7-8 remain in the application. Claims 1 and 7 have been amended. Claims 2 and 5-6 have been cancelled.

In item 2 on page 2 of the above-identified Office action, claim 1 has been objected to because of an informality. Appropriate correction has been made.

In items 3-4 on page 3 of the above-identified Office action, claims 5-6 have been objected to under 37 CFR 1.75 as being a substantial duplicate of claims 3-4, respectively. Claims 5-6 have been cancelled.

In item 5 on pages 4-5 of the above-mentioned Office action, claims 1, 3, and 5 have been rejected as being anticipated by Ahmad (US Pat. No. 6,037,639) under 35 U.S.C. § 102(e).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a silicon oxide passivation layer disposed on said side walls of said gate; and
>
> an insulating silicon nitride spacer disposed on said silicon oxide passivation layer, said spacer acting as an oxidation barrier;
>
> said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below at least one of said side walls adjacent said conductive regions.

Ahmad discloses a method for producing a transistor as shown in Fig. 5 thereof, in which a polysilicon gate 112 is formed on top of a gate oxide 108. The side walls of the gate are disposed adjacent conductive regions 118. A layer 126 is formed on the side walls of the gate by oxidation of the gate, on which a silicon oxide spacer 136 is formed (see column 5, lines 18-19). Then, a cap layer 138 of silicon nitride or silicon oxide is formed on the whole surface.

In contrast, according to claim 1 of the instant application, a silicon oxide passivation layer is disposed on the side walls of the gate and subsequently a silicon nitride spacer is disposed on the silicon oxide passivation layer.

First of all, Applicants would like to highlight the difference between a spacer and a passivation layer: a passivation layer is quite thin as its only purpose is to passivate the respective layer on which it is applied. The dimension of a spacer, in contrary, is not negligible as the purpose of the spacer is to provide a space, e.g. to protect the region under the spacer from implantation.

The Examiner refers to the reference number 136 in Ahmad as the equivalent of the silicon oxide passivation layer of the invention of the instant application, and the reference number 138 in Ahmad as the equivalent of the insulating silicon nitride spacer of the invention of the instant application. However, the spacer 136 in Ahmad is not an oxide passivation layer, but a spacer. A person skilled in the art would know that not every isolating layer or part of a layer which extends vertically along the gate is a passivation layer. Furthermore, it is quite clear from Fig. 5 and the respective description of Ahmad that the spacer 136 is adjacent the layer 126. Hence, the reference number 136 of Ahmad cannot be equated with the passivation layer of the invention of the instant application.

Moreover, a person skilled in the art would surely not consider a layer which covers a whole surface as being a spacer. The layer 138 does not fulfill the above-mentioned object of a "spacer." Therefore, it is incorrect to consider the layer 138 of Ahmad as being a nitride spacer. Furthermore, the cap layer 138 is not disposed on a silicon oxide passivation layer, but on the spacer 136.

As already discussed in the response dated August 29, 2002, the MOS-transistor according to the invention of the instant application provides a number of advantages. The fact that the thickened area is positioned adjacent the conductive regions is important to achieve the desired reduction of the leakage current, the so-called GIDL (Gate Induced Grain Leakage). The thickening of the gate oxide (2) in the regions (5) results in a better insulation between the gate and the conductive region thereby reducing the leakage current. A reduced degree of leakage current between the conductive region and the gate results in a prolonged information retention time in single-transistor memory cells (see page 3, lines 1-7 of the specification of the instant application).

Furthermore, according to the invention of the instant application the insulating spacer is formed of silicon nitride. This enables the structuring of a self-aligned

contact, for instance in a DRAM array, which allows the required minimal distance between two gates in such an array to be further reduced. With reference to the transistors shown in Figs. 3 and 4 of the instant application, it is clear that after the transistors shown therein have been formed, they still need to be contacted, for instance by a bit line. This is usually achieved by depositing an insulating layer made of silicon oxide onto the transistors shown in Figs. 3 or 4 and subsequently etching vias into the silicon oxide insulating layer.

If the side wall spacer in the transistor is made of silicon oxide, great care must be taken to ensure that the openings in the etching mask used to form the vias are spaced at a sufficient distance from the side wall spacers. Otherwise, these spacers would also be etched away during the via etch, exposing the side walls of the gate. Lithographic masks can only be produced within a certain level of exactness and the minimal distance which has to be observed between the via and the side wall spacer is determined by this degree of exactness. Consequently, this distance must include a safety margin taking into account the possible deviation of the position of the via due to the use of the photolithographic etching mask.

This problem is avoided by the use of a silicon nitride spacer to protect the side walls of the gate stack. The etching of vias in the silicon oxide insulating layer is selective for silicon oxide. The silicon nitride layer spacer is not etched by this process. Consequently, there is no need for the safety margin and the distance between the gate and the via and the distance to the next gate in the array can be further reduced.

Even if, for the sake of argument, the layer 138 of Ahmad could be considered to be a nitride spacer, the layer 138 is not formed on a passivation layer, but on a further silicon oxide spacer 136. Accordingly, Ahmad basically uses two spacers which increases the lateral dimension of the gate stack considerably and thereby reduces the integration density of the memory cells. Furthermore, producing additional spacers requires at least one additional lithographic step which increases the cost of the production process of the transistor considerably.

In contrast to Ahmad, the MOS transistors according to the invention of the instant application combine a reduced leakage current with reduced space requirements and therefore have a higher level of integration on a substrate. Ahmad does not provide any hint toward this direction.

Clearly, Ahmad does not show "a silicon oxide passivation layer disposed on said side walls of said gate; and an insulating silicon nitride spacer disposed on said silicon oxide passivation layer, said spacer acting as an oxidation barrier," as recited in claim 1 of the instant application.

Claim 1 is, therefore, believed to be patentable over Ahmad and since claim 3 is dependent on claim 1, it is believed to be patentable as well. Claim 5 has been cancelled.

In item 7 on page 6 of the above-mentioned Office action, claims 4 and 6 have been rejected as being unpatentable over Ahmad in view of Sun et al. (US Pat. No. 5,612,249) under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claim 4 is dependent on claim 1, it is believed to be patentable as well. Claim 6 has been cancelled.

In item 8 on page 7 of the above-mentioned Office action, claim 7 has been rejected as being unpatentable over Ahmad and Sun et al. and further in view of Krautschneider (US Pat. No. 5,854,500) under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claim 7 is ultimately dependent on claim 1, it is believed to be patentable as well.

In item 9 on page 8 of the above-mentioned Office action, claim 8 has been rejected as being unpatentable over Ahmad in view of Krautschneider under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claim 8 is dependent on claim 1, it is believed to be patentable as well.

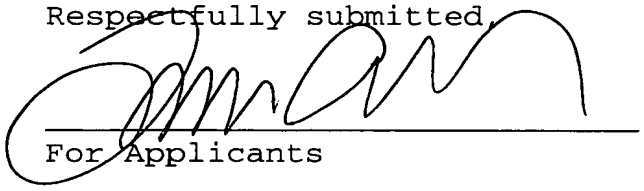
In view of the foregoing, reconsideration and allowance of claims 1, 3-4, and 7-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to

the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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